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I. Earned Degrees

Degree	*School*	*Date*	*Major*
B.S.	Pratt Institute (Honors)	1985	EE
M.S.	University of California at Berkeley	1990	EECS
Ph.D.	University of California at Berkeley	1992	EECS

II. Employment

1985 - 1986	Member of Technical Staff, AT&T Bell Laboratories.
1992 - 1994	Research Staff Member, IBM T. J Watson Research Center.
1993 - 1994	Adjunct Professor, EE Dept., Polytechnic University.
1994 - 1997	Assistant Professor, School of ECE, Purdue University.
1997 - 1998	Dr. Martin L. King Visiting Professor, EECS Dept., MIT.
1998 - 2000	Assistant Professor, School of ECE, Cornell University.
2000 - 2005	Associate Professor, School of ECE, Cornell University.
2006 - 2012	Motorola Foundation Professor, School of ECE, Georgia Tech
2012 - 2015	Professor, Morgan State University, ECE Dept.
2016 - Present	IoT Security Endowed Chair, Morgan State University, ECE Dept.

III. Teaching

A. Ph.D. Student Guidance

Purdue University School of Electrical and Computer Engineering

Name	**Ph.D. Dissertation Title**	**Graduation Date**	**Place of Employment**
1. Sei-Hyung Ryu	Development of CMOS Technology for Smart Power Application in Silicon Carbide	Spring 1997	Cree Inc., Durham, NC
2. Jian-Song Chen	Analog Integrated Circuit Technology using 6H Silicon Carbide CMOS Technology	Fall 1997	Texas Instruments Inc., Dallas, TX
3. Man Pio Lam	Development of Submicron CMOS in 6H-SiC	Summer 1998	Hitachi Corp., Santa Clara, CA

Cornell University School of Electrical and Computer Engineering

Name	Ph.D. Dissertation Title	Graduation Date	Place of Employment
1. Andrew Atwell	Silicon Carbide MEMS Devices for Harsh Environments	Fall 2002	Institute of Defense Analysis, Alexandria, VA
2. Eskinder Hail	Monolithic Integration of Electronics and MEMS in Silicon Carbide for Use in Harsh Environments	Fall 2002	IBM, Austin, TX
3. Ce Li	Silicon Carbide Nonvolatile Memory for Harsh Environments	Summer 2003	Patent Attorney, Washington, DC
4. Mihaela Balsenu	Silicon-on-Silicon System Packaging	Summer 2003	Applied Materials Inc., Santa Clara, CA
5. Swaroop Kumar Kommera	Seamless Tiling of Silicon Dies for Micro-Display Applications and Novel Structures for On-chip Power and Ground Distribution	Fall 2003	IBM, Burlington, VT
6. Paul Ampadu	An Energy Efficient Approach to 3G Turbo Decoding	Spring 2004	University of Rochester, ECE Dept., Rochester, NY
7. David Fried	The Design, Fabrication, and Characterization of Independent Gate FinFETs	Spring 2004	IBM, T.J. Watson Research Center, Yorktown Heights, NY
8. J. C. Zhan	Design of Emitter Degenerated Voltage Controlled Oscillators	Summer 2004	Intel Corp., Hillsboro, OR
9. Sean Welch	Design and Analysis of an Improved Clocking Methodology for Next-generation	Summer 2004	Intel Corp., Hudson, MA

	Physically Aware Synchronous Architectures		
10. Ian Rippke	Design and Analysis of an Improved Clocking Methodology for Next-generation Physically Aware Synchronous Architectures	Spring 2005	Agilent, Santa Clara, CA
11. Kyle Maurice	The Modeling and Design of a Multi-Standard Frequency Synthesis System	Spring 2005	Intel Corp., Hillsboro, OR
12. Franklin Baez	Low Power Analog Baseband for WCDMA Wireless Receivers	Spring 2005	IBM Corp., East Fishkill, NY
13. Drew Guckenberger	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Spring 2005	Luxtera Inc., Carlsbad, CA
14. Daniel Kucharski	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Spring 2005	Luxtera Inc., Carlsbad, CA
15. Brian Welch	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Fall 2006	Luxtera Inc., Carlsbad, CA
16. Yanxin Wang	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Fall 2006	Luxtera Inc., Carlsbad, CA
17. Javier Alvarado	Low-power Integrated	Fall 2007	Raytheon

	Silicon Optical Receiver Design for High-Performance Datalinks		
18. Pukar Malla	Cognitive Delta-Sigma ADC Design for Smart Power Adaptive Digitally Enhanced Receivers	Fall 2007	Silicon Valley, CA

Georgia Tech School of Electrical and Computer Engineering

Name	**Ph.D. Dissertation Title**	**Graduation Date**	**Place of Employment**
1. Tonmoy Mukherjee	High-Performance, Robust, Multi-Gigabit Wireline Design	May 2010	National Semiconductor Norcross, GA
2. Jihwan Kim	CMOS PA Design	May 2011	Intel Corp., Hillsboro, OR
3. Eung Kim	CMOS Switch Design	May 2011	Qualcomm Inc., San Diego, CA

B. Undergraduate Student Guidance

Name	*Research Topic*	*Length of Time Advised*
1. Elijah Lowe	Baseband Processor Design	Summer 2006
2. Joseph Robertson	Data Acquisition System Des. & Syn.	Summer 2007
3. Alexander Johnson	Feedforward Equilizers	Summer 2010
4. Yancy Diaz Mercado	Adaptive Equalization of Fib.	Summer 2010

C. Other Teaching Activities

- Dr. Kornegay has worked with Dr. Joyce Weinsheimer of the Center for Enhancement of Teaching and Learning to improve teaching effectiveness and student survey responsiveness in Spring 2009.

IV. Scholarly Accomplishments

A. Books and Parts of Books

K. T. Kornegay, "Chip and Board Testing," Chapter 14 in book entitled "Anatomy of a Silicon Compiler," Edited by R.W. Brodersen, *Kluwer Academic Publishers*, Norwell, MA, pp.187-196, 1992.

C. Refereed Publications

*The boldface font is used to identify co-authors who were doctoral students advised by Prof. Kornegay.

Journal Publications

[J1] K. T. Kornegay and R. W. Brodersen, "Integrated Test Solutions for a System Design Environment," *J. VLSI Design*, vol. 1, pp. 345-357, Jan. 1994.

[J2] **S. Ryu** and K. T. Kornegay, "Design and Fabrication of Depletion Load NMOS Integrated Circuits in 6H-SiC," *Proc. Int. Conf. Silicon Carbide and Related Mater*., pp. 789-792*,* Feb.1996.

[J3] K. T. Kornegay and K. Roy, "Structured Test Methodologies and Test Economics for Multichip Modules," *IEEE Trans. Compon. Packag. Technol.*, vol. 19, pp. 195-202, Feb. 1996.

[J4] **J. Chen** and K. T. Kornegay, "Class AB CMOS Power OPAMP with Stable Voltage Gain over a Wide Temperature Range," *IEE Proc., Circuits Devices Syst.,* vol. 144, pp. 22-28*,* Feb.1997.

[J5] **M. P. Lam**, K. T. Kornegay, J.A. Cooper, Jr. and M. R. Melloch, "Planar 6H-SiC MESFETs with Vanadium Implanted Channel Termination," *IEEE Trans. Electron Devices,* vol. 44, pp. 907-910, May 1997.

[J6] **S. Ryu**, K. T. Kornegay, J.A. Cooper, Jr., and M. R. Melloch, "Monolithic CMOS Digital Integrated Circuits in 6H-SiC Using an Implanted P-Well Process," *IEEE Electron Device Lett.,* vol. 18, pp. 194-196, May1997.

[J7] **S. Ryu**, K. T. Kornegay, J. A. Cooper, Jr., and M R. Melloch, "Digital CMOS ICs in 6H-SiC Operating on a 5V Power Supply," *IEEE Trans. Electron Devices,* vol. 45, pp. 45-53*,* Jan. 1998.

[J8] **M. P. Lam**, M. K. Das, J. N. Pan, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Effects of Nitrogen Implant Activation on the SiC/SiO_2 Oxide Interface of 6H-SiC Self-Aligned Mosfets," *IEEE Trans. Electron Devices,* vol. 45, pp. 565-567*,* Feb. 1998.

[J9] **J. Chen** and K. T. Kornegay, "Design of a Process Variation Tolerant CMOS OPAMP in 6H-SiC Technology for High Temperature Operation," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 1159-1171, Nov. 1998.

[J10] I. Hong, D. Kirovski, K. T. Kornegay and M. Potkonjak, "High-Level Synthesis Techniques for Test Pattern Execution," *Integ. VLSI J.,* vol. 25, pp. 161-180, Nov. 1998.

[J11] **J. Chen**, K. T. Kornegay, and S. Ryu, "A Silicon Carbide CMOS Intelligent Gate Driver Circuit with Stable Operation over a Wide Temperature Range," *IEEE J. Solid-State Circuits,* vol. 34, pp. 192-204, Feb. 1999.

[J12] **M. P. Lam** and K. T. Kornegay, “Recent Progress in 6H-SiC CMOS Devices for Smart Power Applications,” *IEEE Trans. Electron Devices*, vol. 46, no. 3, pp. 546-554, March 1999.

[J13] **M. P. Lam** and K. T. Kornegay, "Punchthrough Behavior in Short Channel 6H-SiC MOS Transistors at Elevated Temperatures,” *IEEE Trans. Compon. Packag. Technol.,* vol. 22, pp. 433-438, Sept. 1999.

[J14] G. L. Katulka, D. J. Hepner, B. Davis, E. Irwin, M. Ridgley, and K. T. Kornegay, “Characterization of Silicon Carbide and Commercial-Off-The-Shelf (COTS) Components for High-g Launch and EM Applications,” *IEEE Trans. Magnetics*, vol. 37, pp. 248-251, Jan. 2001.

[J15] **A. Atwell**, R. Okojie, K. Kornegay, S. Roberson and A. Beliveau, “Simulation and Validation of Bulk Micromachined 6H-SiC High-G Piezoresistive Accelerometers,” *IEEE Sens. Actuators A*, *Phys.*, vol. 104, pp. 11-18, Feb. 2003.

[J16] **C. Li**, J. S. Duster and K. Kornegay, “A Nonvolatile Memory Device in 6H-SiC for Harsh Environment Applications,” *IEEE Electron Device Lett.,* vol. 24, pp. 72-74, Feb. 2003.

[J17] **D. M. Fried**, J. S. Duster and K. T. Kornegay, “Improved Independent Gate N-type FinFET Fabrication and Characterization,” *IEEE Electron Device Lett.*, vol. 24, pp. 592-594, Sept. 2003.

[J18] **J. C. Zhan**, K. Maurice, J. S. Duster and K. T. Kornegay, “Analysis and Design of Negative Impedance LC Oscillators Using Bipolar Technology,” *IEEE Trans. Circuits Syst. I*, vol. 50, Nov. 2003.

[J19] **D. M. Fried**, J. S. Duster, and K. T. Kornegay, “High Performance P-Type Independent-Gate FinFETs,” *IEEE Electron Device Lett.*, vol. 25, pp. 199-201, April 2004.

[J20] **J. C. Zhan**, J. S. Duster and K. T. Kornegay, “Design of Negative Impedance LC Oscillators using Bipolar Technology,” *IEEE J. Solid-State Circuits*, vol. 39, pp. 2062-64, Nov. 2004.

[J21] **D. Kucharski** and K. T. Kornegay, “Jitter Considerations in the Design of a 10 Gb/s Automatic Gain Control Amplifier,” *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 590-597, Feb. 2005.

[J22] **J. C. Zhan**, J. S. Duster, and K. T. Kornegay, “A high f_{osc}/f_T Ratio VCO in SiGe BiCMOS Technology,” *IEEE Microw. Wirel. Comp. Lett.*, vol. 15, pp. 149-161, March 2005.

[J23] **D. Guckenberger**, C. Shuster, Y. Kwark, and K. T. Kornegay, “On-chip Crosstalk Mitigation of Densely Packed Striplines using via Fence Enclosures,” *Electron. Lett.*, vol. 41, pp. 412-414, March 2005.

[J24] **D. Guckenberger** and K. T. Kornegay, “Design of a Distributed Amplifier and Oscillator using Closed-packed Interleaved Transmission Lines,” *Special Issue on the IEEE 2004*

BCTM, *IEEE J. Solid-State Circuits,* vol. 40, pp. 1997-2007, Oct. 2005.

[J25] **B. Welch**, K. Kornegay, H. Park, and J. Laskar, "A 20 GHz Low Noise Amplifier with Active Balun in a 0.25 μm SiGe BICMOS technology," *Special Issue on the IEEE 2004 CSICS*, *IEEE J. Solid-State Circuits,* vol. 40, pp.2092-2097*,* Oct. 2005.

[J26] **D. Kucharski** and K. Kornegay, "A 2.5V 43-45 Gb/s CDR Circuit and 50 Gb/s PRBS Generator in SiGe using a Low Voltage Logic Design Family," *Special Issue on the IEEE 2005 BCTM*, *IEEE J. Solid-State Circuits,* vol. 41, pp. 2154-2165, Sept. 2006.

[J27] **T. S. Mukherjee**, A. K. Sutton, K. T. Kornegay, R. Krithivasan, J. D. Cressler, G. Niu, and P. W. Marshall, "A Novel Circuit-Level SEU Hardening Technique for High-Speed SiGe HBT Logic Circuits," *IEEE Trans. on Nuclear Sci*., vol. 54, pp. 2086-2091, Dec. 2007.

[J28] **P. Malla**, H. Lakdawala, R. Naiknaware, S. Krishnamurthy, and K. Kornegay, "Delta Sigma ADC Design Considerations for WiFi/WiMAX Receivers," *Analog Integrated Circuits and Signal Processing Journal*, 2008.

[J29] **J. Kim**, K.T. Kornegay, J.A. Alvarado, C.H. Lee, and J. Laskar, "W-band double-balanced down-conversion mixer with marchand baluns in silicon-germanium technology," *Electronics Letters*, vol.45, no. 16, pp. 841-843, July 2009.

[J30] **J. Kim**, H. Kim, Y. Yoon, K. H. An, W. Kim, C.-H. Lee, and K. T. Kornegay, "A Linear Multi-Mode CMOS Power Amplifier with Discrete Resizing and Concurrent Power Combining Structure, to appear in, *Special Issue on the IEEE 2010 RFIC, IEEE J. Solid-State Circuits*, June 2011.

Refereed Conference Publications

[C1] A. Stolzle, S. Narayanaswamy, K. T. Kornegay, et al., "A VLSI Implementation for the Wordprocessing Subsystem of a Real-Time Large Vocabulary Continuous Speech Recognition System," *Proc*. *IEEE CICC*, 1989, pp.15-18.

[C2] K. T. Kornegay and R. W. Brodersen, "A Test Controller Board for TSS," *Proc*. *Great Lakes Symp. VLSI*, 1991, pp. 38-42.

[C3] K. T. Kornegay and R. W. Brodersen, "An Architecture for a Reconfigurable IEEE 1149.1,2, or 5 Master Controller Board," *Proc*. *IEEE Int. Test Conf.*, 1992, pp. 978-983.

[C4] M. Potkonjak, S. Dey and K. T. Kornegay, "Techniques for Implementation of At-Speed Testable, High Performance, and Low Cost Linear Designs," presented at the 1995 *Int. Test Synth. Workshop*, May 1995.

[C5] **S. Ryu** and K. T. Kornegay, "Design and Fabrication of Depletion Load NMOS Integrated Circuits in 6H-SiC," *Proc. Int. Conf. Silicon Carbide and Related Mater.*, 1995, pp. 475-476.

[C6] M. Potkonjak, S. Dey and K. T. Kornegay, "Techniques for Implementation of At-Speed Testable, High Performance and Low Cost Linear Design," *Proc. VLSI Signal Processing*, 1995, pp. 227-236.

[C7] K. T. Kornegay and K. Roy, "Integrated Test Solutions and Test Economics for MCMs," *Proc. IEEE Int. Test Conf.,* 1995*,* pp. 193-201.

[C8] **M. P. Lam**, K. T. Kornegay and J. A. Cooper, Jr., "A Highly Resistive Layer in Silicon-Carbide Obtained by Vanadium Ion Implantation," *Proc. Int. Semicond. Device Res. Symp.*, 1995, pp. 517-519.

[C9] L. Chiou, K. M. Mahoney, K. T. Kornegay and A. M. Weiner, "High-Speed Switching Circuits for Ultrafast Optical Processing," *Proc. IEEE Int. Symp. Circuits Syst., 1996,* pp. 109-112.

[C10] **M. P. Lam**, K. T. Kornegay, J.A. Cooper, Jr., and M. R. Melloch, "Ion Implantation Technology for 6H-SiC MESFET Digital ICs," *DRC Dig.,* 1996*,* pp. 158-159.

[C11] **J. Chen** and K. T. Kornegay, "Design of a Silicon Carbide CMOS Power OPAMP for Stable Operation at Elevated Temperatures," *Proc. IEEE ISCAS,* 1997*,* pp. 157-160.

[C12] **S. Ryu**, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "6H-SiC Digital CMOS ICs Operating on a 5V Power Supply," *DRC Dig.*, 1997, pp. 38-39.

[C13] **M. P. Lam**, K .T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Effects of Implant Anneal on Oxide Interface of Self-Aligned Mosfets in 6H-SiC," *EMC Dig. Tech. Papers*, 1997, pp. 27-28.

[C14] **J. Chen** and K. T. Kornegay, "Design of a Silicon Carbide Smart Power Switch with Stable Operation over a Wide Temperature Range," *Proc. IEEE Midwest Symp. Circuits Syst.*, 1998, pp. 123-126.

[C15] **J. Chen** and K.T. Kornegay, "A constant input gm and rail-to-rail CMOS OPAMP using 6H SiC CMOS technology," *Proc. IEEE Int. Symp. Circuits Syst.*, 1998, pp. 241-244.

[C16] K.T. Kornegay, "Design Issues in Power Electronics Building Block (PEBB) System Integration," *Proc. IEEE Computer Society Workshop on VLSI*, 1998, pp. 48-52.

[C17] **J. Chen**, S. Ryu and K. T. Kornegay, "High Temperature Mixed-Signal ICs using Silicon Carbide CMOS Technology," in *Proc. Int. High Temp. Electron. Conf.*, 1998, pp. 292-295.

[C18] **J. Chen**, S. Ryu and K. T. Kornegay, "A Silicon Carbide CMOS Intelligent Gate Driver Circuit," *IEEE Industry Appl. Society Annual Meeting Dig.*, 1998, pp. 963-966.

[C19] K. T. Kornegay, "Submicron Silicon Carbide CMOS for Smartpower Applications," *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 1999, pp. 297-300.

[C20] K. T. Kornegay, "Silicon Carbide CMOS Technology for High Temperature Applications," *NASA/JPL Conf. Electron. Extreme Environ.*, 1999, pp. 14-18.

[C21] E. Eshun, C. Taylor, M. G. Spencer, K. T. Kornegay, I. Furgureson, and A. Gurray, "Homo-Epitaxial and Selective Area Growth of 4H and 6H Silicon Carbide using A Resistively Heated Vertical Reactor," *Proc. Symp. Bandgap Semicond. High-Power, High-Freq. High-Temp. Appl.*, 1999, pp. 173-179.

[C22] C. Thomas, C. Taylor, J. Griffen, M. G. Spencer, K. T. Kornegay, M. Capano, and S. Rendakova, "Annealing of Ion Implantation Damage in SiC using A Graphite Mask," in *Proc. Symp. Bandgap Semicond. High-Power, High-Freq. and High-Temp. Appl.*, 1999, pp. 45-50.

[C23] K. T. Kornegay, G. Qu, and M. Potkonjak, "Quality of Service and System Design," *Proc. IEEE Computer Society Workshop on VLSI*, 1999, pp. 112-117.

[C24] **S. M. Welch** and K. T. Kornegay, "Improved Synchronization Methodologies for High Performance Digital Systems," Invited Paper, *Proc. IEEE Computer Society Workshop on VLSI*, 2000, pp. 61-66.

[C25] **A. R. Atwell**, J. S. Duster, K. T. Kornegay, and R. S. Okojie, "A Novel CMOS-compatible Deep Etching Process for Silicon Carbide using Silicon Shadow Masks," *Proc. EMC*, June 2000.

[C26] **E. Hailu** and K. T. Kornegay, "Design of a Temperature Independent Current Source for High Temperature Operation," *Proc. Int. High Temp. Electron. Conf.*, May 2000.

[C27] K. T. Kornegay, "Anatomy of an RF Integrated Circuit Design Course," *Proc. IEEE Int. Conf. Microelectron. Syst. Educ.*, 2001, pp. 54-55.

[C28] R. S. Okojie, **A. R. Atwell**, K. T. Kornegay, S. L. Roberson, and A. Beliveau, "Design Considerations for Bulk Micromachined 6H SiC High-G Piezoresistive Accelerometers," *Proc. IEEE Int. Conf. MEMS Dig. Tech. Papers, 2002*, pp. 618-622.

[C29] **E. Hailu**, A.R. Atwell, J. S. Duster, C. Li, M. Balseanu and K. T. Kornegay, "The Monolithic Integration of 6H-SiC Electronics with 6H-SiC MEMS for Harsh Environment Applications," *Proc. Int. Nanotechnol. Conf. Trade Show*, 2003, pp. 270-271.

[C30] **M. Balsanu**, J. S. Duster, and K. T. Kornegay, "Homogeneous Integration of Off the Shelf Si-Based ICs on a Si Substrate," *Proc. Electron. Compon. Technol. Conf.*, 2003, pp.397-402.

[C31] **J.C. Zhan**, K. Maurice, J. S. Duster, and K. T. Kornegay, "Analysis of an Emitter Degenerated LC Oscillator using Bipolar Technologies," *Proc. IEEE ISCAS*, 2003, pp. 669-672.

[C32] **D. Guckenberger** and K. T. Kornegay, "Novel Low-Voltage, Low-Power Gb/s Transimpedance Amplifier Architecture," *Proc. SPIE – Int. Soc. Opt. Eng.,* 2003, pp. 274-285.

[C33] **I. Rippke**, J. S. Duster, and K. T. Kornegay, "A Fully Integrated Single-Chip Handset Power Amplifier in SiGe BiCMOS for W-CDMA Applications," *IEEE RFIC Symp. Dig.*, pp. 667-670, June 2003.

[C34] **D. M. Fried**, E. J. Nowak, J. Kedzierski, J. S. Duster, and K. T. Kornegay, "A Fin-Type Independent-Double-Gate NFET," *Device Res. Conf. Dig.*, 2003, pp. 45-46.

[C35] **D. Guckenberger** and K. T. Kornegay, "Integrated DC-DC Converter Design for Improved WCDMA PA Efficiency in SiGe BiCMOS Technology," *Proc. IEEE ISLPED.*, 2003, pp. 449-454.

[C36] **J.C. Zhan**, J. S. Duster, and K. T. Kornegay, "A 24.5 GHz Emitter Degenerated SiGe Bipolar VCO," *Proc. BCTM*, 2003, pp. 71-74.

[C37] K. T. Kornegay, "60 GHz Radio Design Challenges," *IEEE GaAs IC Symp. Tech. Dig.*, 2003, pp. 89-92.

[C38] **P. Ampadu**, K. Kornegay, "An Efficient Hardware Interleaver for 3G Turbo Decoding," *Proc. IEEE Radio Wirel. Conf.*, 2003, pp. 199-201.

[C39] **D. Guckenberger**, D. Kucharski, J. C. Zhan, and K. T. Kornegay, "A 10 Gb/s Integrated Optical Transceiver," *SRC TECON 2003*, August 2003.

[C40] **D. Guckenberger**, J. D. Schaub, and K. T. Kornegay, "A DC-Coupled Low Power Transimpedance Amplifier for Gb/s Optical Communication Applications," *IEEE RFIC Symp. Dig.*, 2004, pp. 515-518.

[C41] **D. Kucharski** and K. T. Kornegay, "A Low Power 10 Gb/s AGC Optical Postamplifier in SiGe," *IEEE RFIC Symp. Dig.*, 2004, pp. 24-28.

[C42] **F. Baez**, B. A. Minch, J.S. Duster, and K. T. Kornegay, "A 1.5V Class-A 5^{th} Order Log Domain Filter in SiGe Technology," *Proc. IEEE ISCAS,* 2004, pp. 853-856.

[C43] **J. C. Zhan**, J. S. Duster, and K. T. Kornegay, "A Comparative Study of MOS VCO for Low Voltage High Performance Operation," *Proc. IEEE ISLPED,* 2004, pp. 244-247.

[C44] **D. Guckenberger** and K. Kornegay, "Differential Distributed Amplifier and Oscillator in SiGe BiCMOS using Close-Packed Interleaved On-Chip Transmission Lines," *Proc. IEEE BCTM*, 2004, pp. 68-71.

[C45] **J. C. Zhan**, J. S. Duster, and K. T. Kornegay, "A 7.3GHz, 55% Tuning Range Emitter Degenerated Active Inductor VCO," *Proc. IEEE BCTM*, 2004, pp. 60-63.

[C46] **B. P. Welch**, K. T. Kornegay, H. M. Park, and J. Laskar, "A 20GHz Low Noise Amplifier with Active Balun in a 0.25µm SiGe BiCMOS Technology," *IEEE CSIC Symp. Tech. Dig.*, 2004, pp. 141-144.

[C47] **F. Baez**, J. S. Duster, and K. T. Kornegay, "A Low Power 60 dB Programmable Gain Amplifier in SiGe Technology," *Proc. IASTED Conf. Circuits Signals Syst.*, 2004, pp. 477-480.

[C48] **J. Alvarado,** J. S. Duster, and K. T. Kornegay, "An 18.7dB Gain, 2.0dB Noise Figure Low-Noise Amplifier in SiGe Technology for Various 2.4GHz Applications," *Proc. IASTED Conf. Circuits Signals Syst.,* 2004, pp. 537-540.

[C49] **D. Kucharski**, Y. Kwark, **D. Guckenberger**, D. Kuchta, K. Kornegay, M. Tan, C. K. Lynn, and A. Tandon, "A 20Gb/s CMOS VCSEL Driver with Pre-Emphasis and Regulated Output Impedance in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, 2005, pp. 222-223.

[C50] **D. Kucharski** and K. Kornegay, "A 40Gb/s PRBS Generator in SiGe using a Low-Voltage Logic Family," *ISSCC Dig. Tech. Papers*, 2005, pp. 340-341.

[C51] **B. P. Welch**, **J. C. Zhan**, and K. T. Kornegay, "A Family of SiGe Quadrature Oscillators for Microwave Applications," *Proc. IEEE ISCAS,* 2005, pp. 4891-4894.

[C52] **Y. Wang**, J. S. Duster, and K. T. Kornegay, "Design of an Ultra Wide Band Low Noise Amplifier in 0.13µm CMOS," *Proc. IEEE ISCAS*, 2005, pp. 5067-5070.

[C53] **Y. Wang**, J. Duster, K. Kornegay, H. Park, and J. Laskar, "An 18GHz Low Noise High Linearity Active Mixer in SiGe," *Proc. IEEE ISCAS*, 2005, pp. 3243-3246.

[C54] **B. Welch** and K. Kornegay, "Emitter Degenerated Voltage Controlled Oscillators for Operation from 40 to 60 GHz," *Proc. SPIE – Int. Soc. Opt. Eng.,* 2005, pp. 693-700.

[C55] **Y. Wang**, **B. Welch** and K. Kornegay, "An 18 GHz Integrated Double-balanced Direct Down-conversion Mixer and Emitter Degenerated Quadrature VCO in 47GHz f_t SiGe," *Proc. SPIE – Int. Soc. Opt. Eng.,* 2005, pp. 720-729.

[C56] **D. Guckenberger** and K. Kornegay, "CMOS Current Amplifiers Exhibiting AC and DC Current Amplification," *Proc. SPIE – Int. Soc. Opt. Eng.,* 2005, pp. 158-165.

[C57] **D. Kucharski** and K. Kornegay, "A 40GHz 2.1V Static Frequency Divider in SiGe using a Low-Voltage Latch Topology," *IEEE RFIC Symp. Dig.*, June 2005, pp. 461-464.

[C58] **D. Guckenberger**, J. Schuab, **D. Kucharski**, and K. Kornegay, "1V, 10mW, 10Gb/s CMOS Optical Receiver Front End," *IEEE RFIC Symp. Dig.*, 2005, pp 309-312.

[C59] **I. Rippke**, J. Duster, and K. Kornegay, "A Single Chip Variable Supply Voltage Power Amplifier," *IEEE RFIC Symp. Dig.*, 2005, pp 255-258.

[C60] **J.C. Zhan**, J. S. Duster, and K. Kornegay, "A Full Rate Injection Lock 10 Gb/s Clock and Data Recovery Circuit in a 47 GHz f_T SiGe Process," *Proc*. *IEEE CICC*, 2005, pp. 552-555.

[C61] **D. Kucharski** and K. Kornegay, "A 43-45 GB/s Integrated Clock and Data Recovery Circuit in SiGe using Low Voltage Topologies," *Proc. IEEE BCTM*, 2005, pp. 86-89.

[C62] **J.C. Zhan**, J. S. Duster, and K. Kornegay, "A 10 GB/s Injection Lock Clock Recovery Circuit in 47 GHz f_T SiGe Process," *Proc. IEEE BCTM*, 2005, pp. 94-97.

[C63] **J. Alvarado**, J. S. Duster, and K. Kornegay, "Noise Reduction in LNAs using a Conductive Path to Ground in SiGe Technology," *IEEE A-SSCC Dig. Tech. Papers*, 2005, pp. 185-188.

[C64] **J. Alvarado, Jr**., K. T. Kornegay, D. Dawn, S. Pinel, and J. Laskar, "60 GHz LNA using a Hybrid Transmission Line and Conductive Path to Ground Technique in Silicon," *IEEE RFIC Symp. Dig.*, 2007, pp. 685-688.

[C65] **P. Malla**, H. Lakdwawala, R. Naiknaware, S. Krishnamurthy, and K. Kornegay, "Delta Sigma ADC Design Considerations for WiFi/WiMax Receivers*," Proc. IEEE Int'l. Symp. on Signals, Circuits and Systems*, 2007, pp. 1-4.

[C66] **T. S. Mukherjee**, A. K. Sutton, K. T. Kornegay, R. Krithivasan, J. D. Cressler, G. Niu, and P. W. Marshall, "A Novel Circuit-Level SEU Hardening Technique for High-Speed SiGe HBT Logic Circuits," *Proc. IEEE Nuclear and Space Radiation Effects Conf.,* 2007.

[C67] **P. Malla**, H. Lakdawala, R. Naiknaware, S. Krishnamurthy, and K. Kornegay, "ADC Design Considerations for WiFi/WiMAX Receivers," *Proc. IEEE Int'l Symp. on Signals, Circuits, and Systems*, 2007, pp.1-4.

[C68] **P. Malla**, H. Lakdawala, K. Kornegay and K. Soumyanath, "A Digitally Enhanced 2-0 Delta Sigma ADC," *Proc. IEEE Midwest Symp. on Circuits and Systems*, 2007, pp. 940-943.

[C69] **P. Malla**, H. Lakdawala, K. Kornegay, and K. Soumyanath, " A 28mW Spectrum-Sensing Reconfigurable 20 MHz 72db-SNR 70 dB-SNDR DT Sigma Delta ADC for 802.11n/WiMAX Receivers," *ISSCC Dig. Tech. Papers*, 2008, pp. 496-497.

[C70] **J. A. Alvarado**, **J. Kim**, and K. Kornegay, "W-Band SiGe LNA using Enhanced Unilateral Gain Peaking," *IEEE IMS Dig.*, 2008, pp. 289-292.

[C71] **J. Kim**, **J. A. Alvarado**, and K. Kornegay, "A High-Gain W-Band Receiver Front-End in Silicon Germanium Technology," *IEEE RFIC Symp. Dig.,* 2008, pp. 237-240.

[C72] **M. Umer**, M. Sajadieh, and K. T. Kornegay, "A Fast Converging Adaptive Pre-distorter for Multi-Carrier Transmitters," *IEEE International Communications Conference (ICC)*, 2009.

[C73] **T. S. Mukherjee**, D. Howard, J. D. Cressler, and K. T. Kornegay, "A Wide Bandwidth, SiGe Broadband Amplifier for 100 Gb/s Ethernet Applications," *Proc. IEEE ISCAS*, 2009, pp. 1835-1838.

[C74] **T. S. Mukherjee**, M. Umer, and K. T. Kornegay, "Design and Optimization of a 71 Gb/s Injection-Locked CDR," *Proc. IEEE ISCAS*, 2009, pp. 177-180.

[C75] **T. S. Mukherjee,** K. T. Kornegay, "A 25 GHz Wide Tuning Range VCO Design using a 100GHz SiGe Process," *IEEE ISCAS*, 2010.

[C76] J. Kim, H. Kim, Y. Yoon, K. H. An, W. Kim, C.-H. Lee, K. T. Kornegay, and J. Laskar, "A Discrete Resizing and Concurrent Power Combining Structure for Linear CMOS Power Amplifier," *IEEE RFIC Symp. Dig.*, 2010, pp. 387-390.

Presentations

1. "Future Directions of SiC Research at Purdue," *NASA Lewis Research Center*, Cleveland, OH, Nov. 10, 1994.
2. "VLSI Research at Purdue," *Indiana Microelectronics Center*, October 26, 1995.
3. "Design of a High Performance Chip for Scheduling Real-Time Traffic in ATM Networks," *National Semiconductor Corporation*, Santa Clara, CA, March 4-5, 1996.
4. "Design of Smart Power ICs using Silicon Carbide Technology," *IEEE Computer Society VLSI Workshop*, Clearwater Beach, FL, November 5, 1996.
5. "Design of an Ultrafast Optical Processing Chip," *IEEE Computer Society VLSI Workshop*, Clearwater Beach, FL, Nov. 5, 1996.
6. "Development of 6H-SiC CMOS Technology and its Applications to Power Electronic Building Blocks (PEBBs)," *Cornell EE Colloquium Series*, April 8, 1997.
7. "Development of 6H-SiC CMOS Technology and its Applications to Power Electronic Building Blocks (PEBBs)," *Princeton EE Colloquium Series*, May 12, 1997.
8. "Microelectronic Processing of SiC CMOS Devices," *MIT Material Science and Engineering Electronic Materials Seminar*, September 18, 1997.
9. "Development of 6H-SiC CMOS Technology and its Applications to Power Electronic Building Blocks (PEBBs)," *MIT Microsystems Technology Lab VLSI Seminar Series*, October 28, 1997.
10. "Design Issues in Power Electronics Building Block (PEBB) System Integration," *IEEE Workshop on VLSI*, Orlando, FL, April 15,1998.
11. "Recent Advances in Silicon Carbide Circuit Technology," *DARPA Defense Science Research Council Meeting on Harsh Environments*, System Planning Center, Arlington, VA, May 7, 1998.
12. "Integrated Electronics for Harsh Environments," *DARPA MEMS for Harsh Environments Workshop*, Dulles, VA, Oct. 23-24, 1998.
13. "Integrated MEMS for Harsh Environments," Berkeley Sensors and Actuators Center Seminar - University of California at Berkeley, Berkeley, CA, April 12, 1999.

14. “Silicon Carbide Circuit Technology and Applications,” Integrated Circuits Technology and Design Seminar - Stanford University, Palo Alto, CA, May 11, 1999.
15. “Integrated MEMS for Harsh Environments,” MiRC GaTech School of ECE, March 23, 2001.
16. “Integrated MEMS for Harsh Environments,” IT Constellation Seminar, RPI, March 20, 2002.
17. “The Roadmap to Single-Chip WCDMA Transceivers – A Circuit Designer’s Perspective,” Symbol Technologies Distinguished Lecture, Polytechnic University, April 9, 2002.
18. “Integrated MEMS for Harsh Environments,” Distinguished Lecture Series in Nanoelectromechanical Systems, The University of Texas at Arlington, April 17, 2003.
19. “CBCRL Research Highlights,” Columbia University EE VLSI Seminar Series, Dec.15, 2003.
20. “CBCRL Research Highlights,” Analog Devices, Wilmington, MA, July 12, 2004.
21. “High Performance VCO Design using SiGe BiCMOS Technology,” IEEE Electron Devices Society Distinguished Lecture, Raytheon, Tampa, FL, Sept. 29, 2004.

E. Other Scholarly Accomplishments

*****The boldface font is used to identify co-inventors who were students being advised by Prof. Kornegay.

1. J. M. Woodall, K. T. Kornegay and M. G. Spencer, “Incandescent Light Energy Conversion with Reduced Infrared Emission,” U.S. patent no. 5,814,840, issued September 29, 1998.

2. **D. Guckenberger**, K.T. Kornegay, “A Novel Low-Voltage Low-Power Transimpedance Amplifier Architecture,” U.S. patent no. 7,042,295, issued May 9, 2006.

3. **D. Kucharski**, K.T. Kornegay, “Low-voltage high-speed differential logic devices and method of use thereof,” U.S. patent no. 7,098,697, issued August 29, 2006.

4. K.T. Kornegay, et al., “Method for monolithically integrating silicon carbide microelectromechanical devices with electronic circuitry,” U.S. patent no. 7,170,141, issued January 30, 2007.

5. **D. Kucharski**, K. Kornegay, “Extended bandwidth and oscillator using positive current feedback through inductive load,” U.S. patent no. 7,215,914, issued May 8, 2007.

6. K.T. Kornegay, et al., “Method for monolithically integrating silicon carbide microelectromechanical devices with electronic circuitry,” U.S. patent no. 7,615,788, issued November 10, 2009.

V. Service

A. Professional Contributions

Administrative:

- NSF Panel, Electrical, Communications and Cyber Systems Division, Spring 2014.
- NSF CAREER Panel, Electrical, Communications and Cyber Systems Division, Fall 2013.
- National Research Council Assessment Panel of NIST Program – Semiconductor Electronics Panel Member, 2007-2009.
- IEEE Solid State Circuits Society Administrative Committee Member, 2007-2009.
- Organizing Committee, 6th and 7th German-American Symposium on Frontiers of Engineering, National Academy of Engineering.
- AdCom Member, IEEE Electron Device Society Educational Activities Committee, 2000 - present. IEEE Electron Devices Society Distinguished Lecturer, 2000-present.
- IEEE Electron Devices Society AdCom Education Activities Committee, 2000-present.
- Co-Organizer, DARPA Workshop on MEMS for Harsh Environments, 1998.

Technical Program:

- IEEE International Solid State Circuits Conference (ISSCC), 2005 – 2006.
- IEEE Custom Integrated Circuits Conference (CICC), 2005 – 1007.
- IEEE International Symposium on Circuits and Systems (ISCAS), 2004 – present.
- IEEE Bipolar/BiCMOS Circuits Technology Meeting (BCTM), 2004 – 2007.
- IEEE Compound Semiconductor IC (CSICS) Symposium, 2004.
- IEEE Radio Frequency IC (RFIC) Symposium, 2003 – 2006.
- IEEE Computer Society Symposium on VLSI, 2003 – present.
- ACM International Symposium on Low Power Electronics and Design (ISLPED), 2003 - present.
- IEEE International Microwave Symposium, 2003, 2008.
- International Conf. on Microelectronic Systems Education, 2003.
- IEEE Great Lakes Symposium on VLSI, 2003.
- IEEE Sensors, 2002, 2003.
- IEEE Symposium on Power Semiconductors and Devices, 2001-2003.
- IEEE Asian and South Pacific Design Automation Conference,1999.
- IEEE Industry Applications Society Annual Meeting, 1998.
- IEEE International Test Conference, 1993 - 1996.
- IEEE Computer Society Workshop on VLSI, 1995.

Editorial:

- Assoc. Editor, IEEE *TCAS-II*, 2008-2010.
- Editorial Advisory Board of *Science Spectrum Magazine*, 2005.
- Guest Editor, Special Issue of the IEEE *Journal of Solid-State Circuits*: Compound Semiconductor IC Symposium, 2005.
- Editor, IEEE *Electron Device Letters*, 2003-2006.

Campus Contributions:

- Lead Cyber Security Embedded Systems UG/Grad Program for Morgan State University.
- Lead I3P membership for Morgan State University.
- Member, Georgia Tech School of ECE Graduate Student Recruiting Committee, 2009-present.
- Member, Georgia Tech School of ECE Undergraduate Committee, 2006-2009.
- Member, Georgia Electronics Design Center, 2006-present.
- Member, Georgia Tech School of ECE, Microelectronics TIG, 2006-present.

Graduate Student Examination Committees

Name	Proposal Committee	Reading Committee	Thesis Defense Committee
Franklin Bien	Spring 2006		Fall 2006
Ramkuma Krithivasan	Spring 2006		Fall 2006
Jon-Hoon Lee	Fall 2006		
Jinsung Park	Spring 2006		
Sheng-Yu Peng	Fall 2006		
Saikat Sarkar	Spring 2006		Fall 2007
Guillermo Serrano	Fall 2006		Summer 2007
Minsk Ahn	Spring 2007		Fall 2007
Soumya Chandram	Fall 2006		Fall 2007
Philip Jones	Spring 2007		
Banerjee Bhaskar			Fall 2006
Kuo Wei-Min			Fall 2006
Perumana Bevin			Fall 2007

B. Other Contributions

Reviewer, IEEE *Microwave and Wireless Component Letters*, 2002 – present (12 papers)
Reviewer, IEEE *Microwave Theory and Techniques*, 2002 – present (11 papers)
Reviewer, IEEE *Transactions on Circuits and Systems*, 2000 – present (12 papers)
Reviewer, IEEE *Transactions on Electron Devices*, 2000 – present (22 papers)
Reviewer, IEEE *Electron Device Letters*, 1996 – present (24 papers)
Reviewer, IEEE *Journal of Solid-State Circuits*, 1992 – present (31 papers)
Reviewer, National Science Foundation CISE, ENG, ERC, 1995 - present (65 proposals)

Consulting Experience

2015, The Aerospace Corporation
2014, Johns Hopkins Applied Physics Laboratory
2003, Future Trends Forum, Madrid, Spain.
2003, Institute for Defense Analysis, Alexandria, VA.
2001, IBM Communications Research and Development Center, Yorktown Heights, NY.
1998, Irell & Manella LLP, Los Angeles, CA.
1998, DARPA-Defense Science Research Council, Arlington, VA.
1997, Foster-Miller, Waltham, MA.

VI. Grants and Contracts

A. As Investigator (at Cornell University)

Sponsor	Period	Title (PI = Principal Investigator)	Amount
1. DARPA/MARCO	1/1/01 – 12/31/04	CCSS: A Collaborative Multi-University Research Center for Circuits, Systems & Software. 30 PIs from CMU, MIT, Stanford, UC-Berkeley, Columbia, Cornell, Princeton, RPI, and the University of Washington.	$18,747,993 (Kornegay: $380,000)
2. NYSTAR - Alliance for Nanomedical Technologies	8/01-7/02	A Remote Non-invasive Ambulatory Patient Monitoring System	$270,000

B. As Principal and Co-Principal Investigator (1995-1997, Purdue University, 1998-2005, Cornell University, 2005-present, Georgia Tech)

Sponsor	Period	Title	PI/Co-PI	Amount
1. NSF	11/95 - 5/96	A Look at Temperature Dependent Parameters for Digital Circuit Design Considerations using SiC MOSFET Technology	PI	$18,000
2. ONR	3/96 - 2/99	Design and Optimization of a SiC CMOS Process for Smart Power ICs	PI	$400,000
3. National Semiconductor	3/96 - 5/98	Faculty Development Award	PI	$40,000
4. Ballistic Missile Defense Organization	5/96 - 4/97	Instrumentation for Research on High Speed Optical Transmultiplexing and Coding	PI	$119,203
5. NSF	5/96 - 6/98	Hardware Prototyping Capability for a Community Service Projects Course in Electrical and Computer Engineering	PI	$159,310
6. ONR	4/97 - 3/00	Microelectronic Integration and Test of PEBB Control Functions	PI	$300,000
7. Alcoa Foundation	5/98	Software and Hardware Infrastructure for High-Temperature Electronics	PI	$30,000

8. ONR	2/99 - 1/00	Silicon Carbide VLSI Technology	PI	$200,000
9. NSF	7/99 - 6/03	CAREER Award: A Wireless Sensor Instrumentation System for Harsh Environments	PI	$285,000
10. AFOSR	5/99 - 5/01	Stress Studies at High G-Loads using Silicon Carbide Piezoresistive Strain Gauges	PI	$200,000
11. DOE	8/99 - 7/00	Assessment of Silicon Carbide as a Viable Semiconductor for Development of High Temperature Electronics	PI	$15,000
12. Wright Patterson Airforce Base	2/1/00 – 5/18/00	Fabrication of Silicon Carbide Pressure Sensors for Jet Engine Applications	PI	$27,000
13. Digital/Compaq	7/1/00 – 6/30/01	Improved Synchronization Methodologies for High Performance Digital Systems	PI	$30,000
14. IBM Corporation	6/00	Shared University Research Grant for Cornell Broadband Communications Research Laboratory (CBCRL)	PI	$750,000
15. Northrop Grumman	12/1/00 – 12/31/00	Heterogeneous Integration of Silicon on Silicon	PI	$50,000
16. Cadence	6/00	System Design Software (CBCRL Software Donation)	PI	Valued at 10's of millions of dollars
17. Agilent Technologies	1/01	84000 RF IC Test System (CBCRL Equipment Donation)	PI	$1,200,000
18. Cascade Microtech	1/01	8-inch Wafer Probe System (CBCRL Equipment Donation)	PI	$200,000
19. IBM Corporation	5/01	IBM Faculty Award	PI	$40,000
20. IBM Corporation	2/01	Program to support Broadband Communications Research	PI	$130,000
21. NYSTAR-Microelectronics Design Research Center	8/1/01-7/31/02	Mixed-Signal Circuits for 3G WCDMA Applications	PI	$50,000
22. DOD/Arnold Engineering Development Center	10/02-5/04	In-Situ Pressure Measurements for Hypersonic Vehicles	PI	$224,000

23. IBM Corporation	5/02	Faculty Award	PI	$40,000
24. BF Goodrich	6/1/02-5/31/03	Monolithically Integrated MEMS in SiC	PI	$50,000
25. NYSTAR – Microelectronics Design Research Center	8/1/02-7/31/03	Energy Efficient Turbo Decoders	PI	$50,000
26. Agilent Technologies	4/03	University Philanthropic grant: Laboratory for Introductory Course on Broadband Data Transport	PI	$111,000
27. Intel Corporation	4/03	Research Award	PI	$65,000
28. IBM Corporation	6/03	Faculty Award	PI	$25,000
29. Qualcomm Inc.	8/03	Gift to Support CBCRL Research	PI	$200,000
30. Cascade Microtech	12/03	CBCRL Equipment Donation (8-inch Wafer Probe System)	PI	$30,000
31. SiGe Semiconductor	5/03	Power Amplifier Design	PI	$80,000
32. Intel Corporation	12/03	CBCRL Equipment Donation (PCs, PDAs, and Printer)	PI	$30,000
33. Intel Corporation	5/04	Research Grant	PI	$65,000
34. IBM Corporation	6/04	Faculty Award	PI	$40,000
35. Analog Devices Inc.	8/04	Gift to Support CBCRL Research	PI	$50,000
36. Analog Devices Inc.	1/05	Gift to Support CBCRL Research	PI	$40,000
37. Intel Corp.	5/05	Research Award	PI	$65,000
38. IBM Corporation	6/05	Faculty Award	PI	$25,000
39. Qualcomm Inc.	1/06	Gift of Support for GEDC	PI	$30,000
40. IBM Corporation	6/06	Faculty Award	PI	$25,000

41. National Semiconductor Corp.	2/08	Very High-Speed Clock and Data Recovery Systems	PI	$50,000
42. National Semiconductor Corp.	1/09	Very High-Speed Clock and Data Recovery Systems	PI	$40,000
43. Korean Institute of Science & Technology via I&C Technology	1/11-11/13	Agreement on Full Scale Project under International Collaborative R&D Program: Development of a Fully-Digital CMOS Transceiver IC for Mobile D-TV and Wireless Applications	PI	$617,000
44. Army	10/2014	Embedded Mobile Tactical Systems -- Reverse Engineering and Countermeasures	PI	$212,000
45. NSF	4/1/2015-3/31/2018	RISE: Embedded Systems Security via Reverse Engineering and Countermeasures	PI	$999,450
46. Army Research Laboratory	9/25/2015 – 9/24/2020	IDIQ Contract: Design Techniques for Low Power Highly Linear CMOS Transceivers	PI	$3,099,906

VII. Honors and Awards

- 2006 IBM Faculty Award
- Named Science Spectrum Trailblazer by Science Spectrum Magazine, 2005.
- Member Profile Feature in *IEEE Institute* June 2005.
- 2005 Golden Torch Award for Educator of the Year from the National Society of Black Engineers.
- Guest Editor, Special Issue of the IEEE Journal of Solid State Circuits: Compound Semiconductor IC Symposium, 2005.
- 2004 IEEE Bipolar/BiCMOS Circuits and Technology Meeting Best Student Paper Award (Student: D. Guckenberger, Advisor: K. Kornegay).
- Featured in *Science Spectrum* and *US Black Engineer & Information Technology* magazines as one of 50 Most Important Blacks in Research Science, 2004.
- 2004 Menschel Award, Cornell University Provost's Award for Distinguished Scholarship.
- IBM Faculty Award, 2001-2005.
- 2003 IEEE Electron Devices Society George Smith Award Finalist.
- 2003 Device Research Conference Best Student Paper Award (Student: D. Fried, Advisor: K. Kornegay).
- World Champion, 6th International Underwater Vehicle Competition, sponsored by the Association for Unmanned Vehicle Systems Corporation, 2003.
- 3rd Place Winner, Phases 1 and 2, Semiconductor Research Corporation Silicon Germanium (SiGe) Design Challenge, (59 universities competed), 2003.

- Featured at the Chicago Museum of Science and Industry as part of an exhibit showcasing contributions made by African Americans to the field of information technology, 2003.
- Invited Attendee, 5th German-American Symposium on Frontiers of Engineering, National Academy of Engineering, 2002.
- Black Engineer of the Year Award, US Black Engineer Magazine and Lockheed Martin (Sponsors), 2002.
- Defense Sciences Study Group, Institute for Defense Analyses/DARPA, 2002-2003.
- Invited Attendee, 5th Annual Symposium on Frontiers of Engineering, National Academy of Engineering, 1999.
- National Science Foundation CAREER Award, 1996 - 2000.
- MIT Dr. Martin Luther King, Jr. Visiting Assistant Professor, 1997.
- Harold T. Amrine Visionary Award from the National Society of Black Engineers, 1997.
- Elected IEEE Senior Member, 1996.
- National Semiconductor Faculty Development Award (Inaugural Recipient), 1996.
- General Motors Faculty Fellowship, 1995.
- AT&T Bell Laboratories Cooperative Research Fellowship, 1986 - 1992.
- AT&T Scholarship, 1983 - 1986.
- Eta Kappa Nu Electrical Engineering Honor Society.
- Tau Beta Pi Engineering Honor Society.