



MORGANTM
CYBERSECURITY ASSURANCE
AND POLICY CENTER

CAP Center Distinguished Lecture Series

“Overview of the Field Programmable Neural Array (FPNA)” Thursday,

March 5, 2026 || 11:00 AM — 1:00 PM

Communications and Journalism Building — Room 101



Dr. Oluseyi (Seyi) Ayorinde

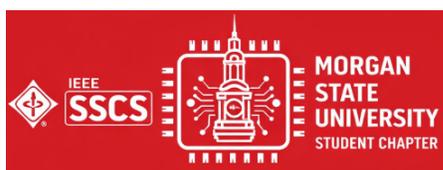
Team Lead – Integrated Circuits
Engineering (ICE) Team

DEVCOM Army Research Lab

Abstract: In this talk, Dr. Ayorinde will provide an overview of both the Combat Capabilities Development Command Army Research Lab (DEVCOM ARL) and the Silicon Integrated Circuit Design (SICD) team within DEVCOM ARL. He will then provide a deep dive into the hardware design of the Field Programmable Neural Array (FPNA), the primary research effort from the SICD team, before discussing ways for students to get involved with research at DEVCOM ARL.

The FPNA is an machine-learning (ML) inference chip designed for low size, weight, and power (SWaP) by operating at power consumption of <1W. The FPNA uses application-specific integrated circuit (ASIC) cores designed for efficient ML inferencing (convolution, fully-connected, etc.) combined with a low-weight, highly-scalable interconnect element for sending data around the chip. Dr. Ayorinde will discuss how each of these circuits work, and how neural networks get mapped to the FPNA using a tool called Neuron Place-and-Route (NPR) that was designed at DEVCOM ARL.

Bio: Dr. Oluseyi (Seyi) Ayorinde is the team lead for the Silicon Technologies Team at the DEVCOM Army Research Lab. He is currently working out of the west coast office in Playa Vista. He received his Ph.D. in Electrical Engineering from the University of Virginia, where he explored generating and configuring custom, sub-threshold FPGA hardware, as well as designed accelerators for ultra-low power Systems-on-Chip (SoCs). He is currently focusing on development of low-power digital circuits for various applications.



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